15. (Amended) A circuit for processing digital data words, comprising:

a multiplier unit for multiplying the digital data words, the multiplier unit having a pipeline in which the word length is adjustable to match the length of the digital data words, the digital data having a length [which varies incrementally] of 8 bits or multiples thereof;

an arithmetic logic unit (ALU) capable of performing arithmetic operations on the digital data words, the ALU being adjustable to match the length of the digital data words;

a register unit having at least two registers for storage of the digital data words; and

a bus structure for transporting the digital data words from and to the multiplier unit, the arithmetic logic unit and the register unit, the bus structure having a plurality of separate buses each having a register connected thereto for transmitting and receiving the digital data words.

19. (Amended) A multiplier unit for multiplying digital data words having a length [which varies incrementally] of 8 bits or multiples thereof, the multiplier unit having a pipeline, the pipeline having a word length which is adjustable to match the length of the digital data words.

Please add the following new claims:

--21. A circuit for processing digital data words, comprising:

a multiplier unit for multiplying the digital data words, the multiplier unit having a pipeline in which the word length is adjustable to match the length of the digital data words, the digital data having a length of 8 bits or multiples thereof;

an arithmetic logic unit (ALU) capable of performing arithmetic operations on the digital data words, the ALU being adjustable to match the length of the digital data words;

a register unit having at least two registers for temporary storage of the digital data words; and

a bus structure for transporting the digital data words from and to the multiplier unit, the arithmetic logic unit and the register unit, the bus structure including:

a first bus coupled to an output of the multiplier unit for receiving the digital data words therefrom;

a second bus coupled to an output of the arithmetic logic unit for receiving the digital data words therefrom;

third and fourth busses coupled to outputs of the two registers, respectively, for receiving the digital data words therefrom; and

a fifth bus coupled to the inputs of the multiplier unit, the arithmetic logic unit and the register unit for transmitting the digital data words thereto.

22. The circuit for processing digital data words of claim 15, further comprising a shift register unit capable of receiving the digital data words having lengths of 8 bits or multiples thereof, the shift register unit for shifting the digital data words through a distance of 1 to multiples of 8 bits, in one of a left and a right direction and in one of a ~~rotating and a non-rotating manner.~~

23. The circuit as claimed in claim 22, further comprising an instruction register, wherein the bus structure is provided with a plurality of registers and wherein the transport of the integer data words from and to the multiplier unit, the arithmetic logic unit and the register unit is programmable from the instruction register.

24. The circuit as claimed in claim 22 in integrated form.--